Journal of the Korean Physical Society, Vol. 54, No. 5, May 2009, pp. 1848∼1853

Laterally-Trapped-Charge Profiling Based on the Extraction of the Flat-Band Voltage by Using the Optical Substrate Current in Charge Trapping Flash Memory Cells

Kang Seob ROH, Sungwook PARK, Kwan-Jae SONG, Jun-Hyun PARK, Sunyeong LEE, Changmin CHOI, Kichan JEON, So Ra PARK, Tae Yoon KIM, Ji Eun LEE, Sangwon LEE, Jaeman JANG, Dae Hwan KIM and Dong Myong KIM*

School of Electrical Engineering, Kookmin University, Seoul 136-702

(Received 20 February 2008, in final form 29 October 2008)

A novel extraction method for the locally-trapped-charge profiling combined with a new local flat-band voltage (V_{FB}) extraction under optical excitation is proposed. Under optical illumination in metal-oxide-semiconductor field effect transistors (MOSFETs), the substrate current ($I_{sub,photo}$) is abruptly increased at V_{FB} due to a sudden increase in the excess carrier diffusion current. In nitride read-only memory (NROM)-type charge trapping flash (CTF) memory cells, there are multi-step responses in optical substrate current ($I_{sub,photo}$)-gate voltage(V_G) curves because V_{FB} is varied along the channel by the laterally non-uniform profile of electrons trapped in the nitride storage layer. We analyzed the mechanism of $I_{sub,photo}$ and verified it by using integrated systems engineering technology computer aided design (ISE TCAD) simulations. The height of the step is shown to be related to the programmed region and the width is shown to be related to the density of trapped charges. Using this novel method, we investigated laterally-trapped-charge profiling in CTF memory cells.

PACS numbers: 85.30.De, 85.30.Tv
Keywords: SONOS, NROM, CTF, Lateral distribution, Substrate current, Optical response, TCAD

I. INTRODUCTION

As one of the promising next generation electrically erasable programmable read-only memories (EEPROMs), nitride-based charge trapping flash (CTF) memories are under active study. Compared with floating gate-type flash memories, the spatial distribution of traps becomes more important in nitride read-only memory (NROM)-type CTF memories due to the spatially discrete nature of the nitride storage layer. Especially, multi-bit operation per cell based on the localized charge trapping has been extensively investigated using a program/erase (P/E) scheme with channel hot electron injection (CHEI) and band-to-band tunneling-assisted hot hole injection (HHI) [1, 2]. This means that the injection path of electrons and/or holes during P/E operation is laterally localized. Moreover, both the evolution of the lateral charge profile and a mismatch between programmed electrons and erased holes were recently reported to have a critical influence on the retention characteristic with P/E cycling [3]. Therefore, an accurate and simple method for extracting the lateral profile of charges trapped in the nitride storage layer is required for the robust design of flash memory products.

Various lateral profiling techniques have been demonstrated to extract the lateral profile of charges trapped in the nitride storage layer. While Gu *et al.* [4] and Arreghini *et al.* [5] have proposed modified charge pumping (CP) methods, Kumar *et al.* [6] and Lusky *et al.* [7] have combined the experimental CP/DC current-voltage ($I-V$) characteristics and the gate induced drain leakage (GIDL)/subthreshold DC $I-V$ characteristics with the device simulation. Because the electrical stress is inevitably induced during characterization and its accuracy decreases as the channel doping concentration becomes laterally more nonuniform, the conventional CP method is not applicable to extremely scaled nonvolatile flash memories. Also, the separation of the interface trap density and the local flat-band voltage shift is so difficult that many efforts and much time are needed.

In this work, for the first time, a new lateral-charge-profiling technique based on local flat-band voltage (V_{FB}) monitoring by using the optical substrate current (I_{sub}) is proposed and is applied to the extraction of the local charge density in charge-trapping flash memory cells. This method monitors the change in the local V_{FB} to the exclusion of interface state density. Thus, it is suitable for extracting the trapped charge distribution of CTF memory cells. Firstly, we explain the mechanism of photo-generated substrate current I_{sub} in metal-oxide-semiconductor field effect transistors (MOSFETs).

*E-mail: dmkim@kookmin.ac.kr; Fax: +82-2-910-4449

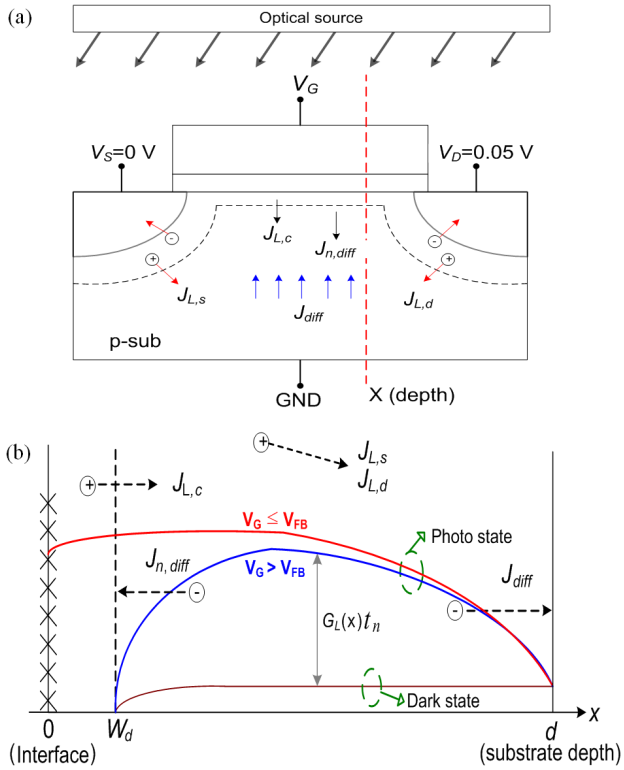

Fig. 1. (a) Schematic diagram illustrating the concept of the proposed technique in an n-type MOSFET. (b) Generated electron distribution in the photo and the dark states, which shows x-cut of (a) (W_d: depletion width, L_n: minority carrier diffusion length, G_L: generation rate and t_n: excess carrier life time).

A step-wise change in the substrate current is shown under optical illumination of the MOSFETs. Secondly, we apply this mechanism to extracting the lateral distribution of the charges trapped in CTF memory devices.

II. NOVEL EXTRACTION METHOD FOR THE LOCAL FLAT-BAND VOLTAGE BY USING AN OPTICAL SOURCE

A schematic diagram illustrating the concept of the proposed technique for extracting of the local flat-band voltage in n-type MOSFETs is shown in Figure 1(a). Under optical excitation at λ = 850 nm and P_{opt} = 1 mW, a photo-induced substrate current density is generated in two regions of the MOSFET substrate. One is at the source/drain space charge region ($J_{L,s}$, $J_{L,d}$) and the other is the channel region ($J_{L,c}$, $J_{n,diff}$, J_{diff}). $J_{L,s}$ and $J_{L,d}$ are photo-induced current densities in the S/D junction, respectively and $J_{L,c}$ is the generation current density in the channel depletion region. $J_{n,diff}$ and J_{diff} are minority carrier diffusion current densities under the channel depletion region. $J_{L,s}$ and $J_{L,d}$ are constant and independent of the applied gate voltage while $J_{L,c}$, $J_{n,diff}$ and J_{diff} depend on the applied gate voltage. In the case of a n-type MOSFET, $J_{L,s}$, $J_{L,d}$ and $J_{L,c}$ (hole current density) and J_{diff} (electron current density) contribute to the total substrate current, as shown in Figure 1(a). We define this as the total photo-induced substrate current $J_{sub,photo}$.

Because the excess carrier generation is exponentially reduced along the substrate, there is a diffusion current to the substrate contact due to nonuniform electrons and holes. Majority carrier hole diffusion is negligible, so there is only a minority carrier electron diffusion current density J_{diff}. In Figure 1(b), the position of the generated electron density's peak concentration is not at the channel surface ($x = 0$) like the generation rate, but is in the middle of the substrate region. In the accumulation region ($V_G \le V_{FB}$), the recombination rate at the channel surface is higher than it is in the bulk region under the influence of the interface trap density. There, the excess minority carrier concentration at the channel surface becomes lower than that in the bulk region. In the case of $V_G > V_{FB}$, a channel depletion region starts to appear. The minority carrier concentration at the depletion-region edge ($x = W_d$) becomes almost zero. Eventually in both cases, there should be a peak concentration position in the middle of the substrate region, as shown in Figure 1(b). Hence, the excess minority carrier diffusion current flows in directions (a) to the channel surface ($J_{n,diff}$) and (b) to the substrate contact (J_{diff}). In the Figure 1(b), J_{diff} is the electron current density contributing to the total substrate current density $J_{sub,photo}$ by a positive number, while $J_{n,diff}$ contributes by a negative number, $J_{L,c}$, $J_{L,s}$ and $J_{L,d}$ are the hole current density contributed by a negative number.

For $V_G < V_{FB}$, the minority carrier concentration at the channel surface, $n(0)$, depends on the surface recombination velocity, S_{front} and it determines $J_{n,diff}$ ($= -qD_n dn(0)/dx$). Figure 1(b) shows $n(0)$ for $V_G < V_{FB}$. When $V_G = V_{FB}$, a channel depletion region starts to appear and the excess minority carrier concentration at the depletion edge abruptly decreases, as shown in Figure 1(b). This means that $J_{n,diff}$ starts to abruptly increase at $V_G = V_{FB}$. Because the positive increased value of $J_{n,diff}$ is the same as the negative decreased value of J_{diff}, the total substrate current ($J_{sub,photo} = J_{L,s} + J_{L,d} + J_{diff} + J_{L,c}$) is increased, as shown in Figure 2. In the simulation, V_G is swept from -3 V to 3 V with the drain bias fixed at $V_D = 0.05$ V. All the other electrodes are grounded. The parameters needed to implement the photo-generation simulation are summarized in Table 1.

The flat-band voltage for the simulated n-type MOSFET ($N_{poly} = 10^{20}$ cm^{-3}, $N_{sub} = 10^{17}$ cm^{-3}) is found to be $V_{FB} = -0.933$ V. In Figure 3(a), $I_{sub,photo}$ is decreased near the flat-band voltage V_{FB} and the mechanism is explained in Figure 3(b). As shown in Figure 3 (b), the minority carrier concentration at the left-end (x = 0) is abruptly reduced when V_G become larger than

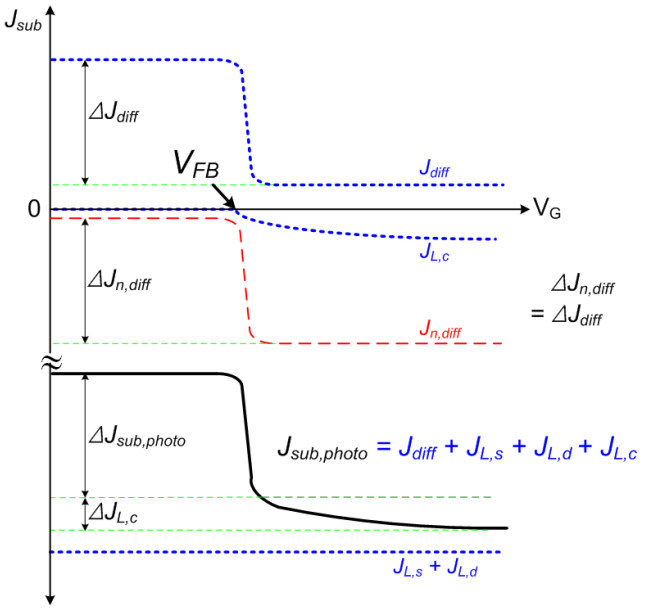

Fig. 2. Schematic diagram of $J_{sub,photo}$ under optical excitation.

Table 1. Parameters for the simulation of photo generation in a MOSFET.

	Device	Parameters
L_g	1.75 μm	L_g: channel length [μm]
H_{sub}	5 μm	H_{sub}: substrate thickness [μm]
t_{ox}	4 nm	t_{ox}: gate oxide thickness [nm]
N_{poly}	10^{20} cm^{-3}	N_{poly}: poly-gate doping concentration [cm^{-3}]
N_{sub}	10^{17} cm^{-3}	N_a: substrate doping concentration [cm^{-3}]

	Optical Source	Parameters
λ(E)	850 nm (1.459 eV)	λ(E): wave length [nm]
α	850 cm^{-1}	α: absorption coefficient [cm^{-1}]
P_{opt}	1 mW (J/s)	P_{opt}: wave power [W/cm^2]

V_{FB}. This means that the gradient of the minority carrier concentration at the depletion edge is abruptly increased, followed by a sudden increase of $I_{sub,photo}$. The V_{FB} point defined by this mechanism is the gate voltage at which $I_{sub,photo}$ start, to have a large increasing gradient. Consequently, $I_{sub} - V_G$ has a sudden increase in the substrate current I_{sub} at $V_G = V_{FB}$ when measuring in an optical illuminated state.

III. LATERAL PROFILING OF TRAPPED CHARGES IN CTF MEMORY CELLS

If V_{FB} is nonuniform along the channel length, caused by a laterally nonuniform profile of electrons trapped in

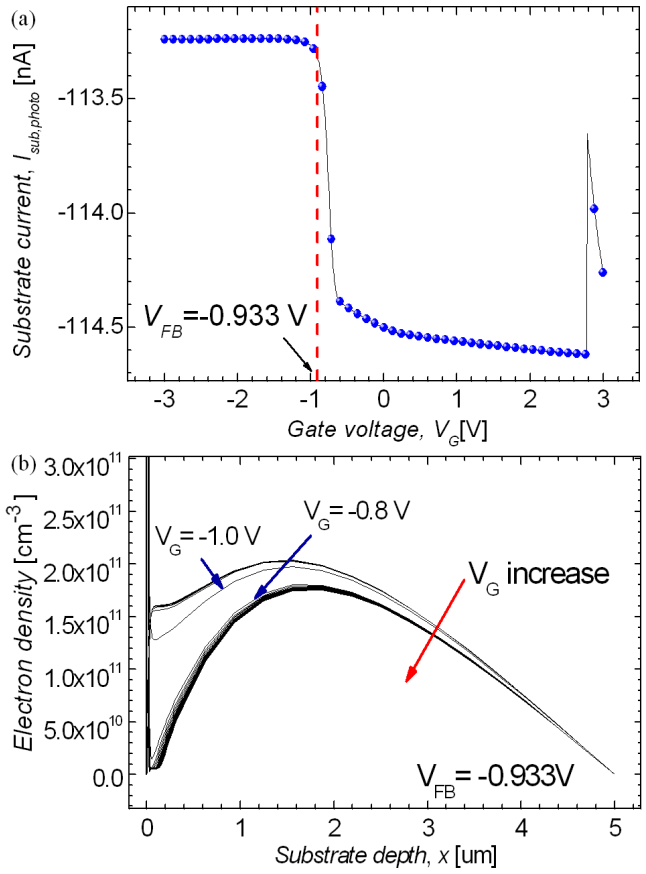

Fig. 3. (a) Simulation results of $I_{sub,photo}$ versus V_G. (b) Simulation data, for the spatial electron density under an optical excitation state by obtained using the ISE TCAD tool. [8]

the nitride storage layer as shown in Figure 4(a), multi-steps in the $I_{sub} - V_G$ curve are expected to be observed, as shown in Figure 4(b). The reason for these multi-steps is that $I_{sub,photo1}$ under the non-program region is abruptly increased at V_{FB1} and $I_{sub,photo2}$ under the program region is increased at V_{FB2}. This means that the multi-step-like substrate current has information on the local flat-band voltage $V_{FB}(x)$. As the density of the trapped electron charges increases, the width of the second step, which is induced by trapped charges, shifts to the right. As the distribution length of trapped charges at fixed channel length, L_{ch}, becomes longer, the height of the second step becomes more pronounced. The trapped charge density, $Q_{nit}(x)$ and the distribution length, x, are described by

$$Q_{nit}(x) = \Delta V_G(x) \cdot C_{ONO}, \tag{1}$$

$$x = \frac{\Delta J_{sub,photo2}}{\Delta J_{sub,photo1} + \Delta J_{sub,photo2}} \cdot L_{ch}, \tag{2}$$

where $\Delta J_{sub,photo1}$ is the total variation of $J_{sub,photo}$ and $\Delta J_{sub,photo2}$ is the variation of $I_{sub,photo}$ under the program region, as shown in Figure 4(b).

Table 2. Parameters for the simulation of photo generation in a CTF memory cell.

	Device	Parameters
L_g	1.75 μm	L_g: channel length [μm]
H_{sub}	5 μm	H_{sub}: substrate thickness [μm]
O/N/O	4 nm / 4 nm / 4 nm	O/N/O: top oxide / nitride / bottom oxide thickness [nm]
N_{poly}	10^{20} cm^{-3}	N_{poly}: poly-gate doping concentration [cm^{-3}]
N_a	10^{17} cm^{-3}	N_a: substrate doping concentration [cm^{-3}]
L_{prog}	0/5 $L_g \sim$ 5/5 L_g	L_{prog}: program region length [μm]
N_{nit}	10^{19} cm^{-3}	N_{nit}: volume charge density [cm^{-3}]

	Optical Source	Parameters
λ(E)	850 nm (1.459 eV)	λ(E): wave length [nm]
α	850 cm^{-1}	α: absorption coefficient [cm^{-1}]
P_{opt}	1 mW (J/s)	P_{opt} : wave power [W/cm^2]

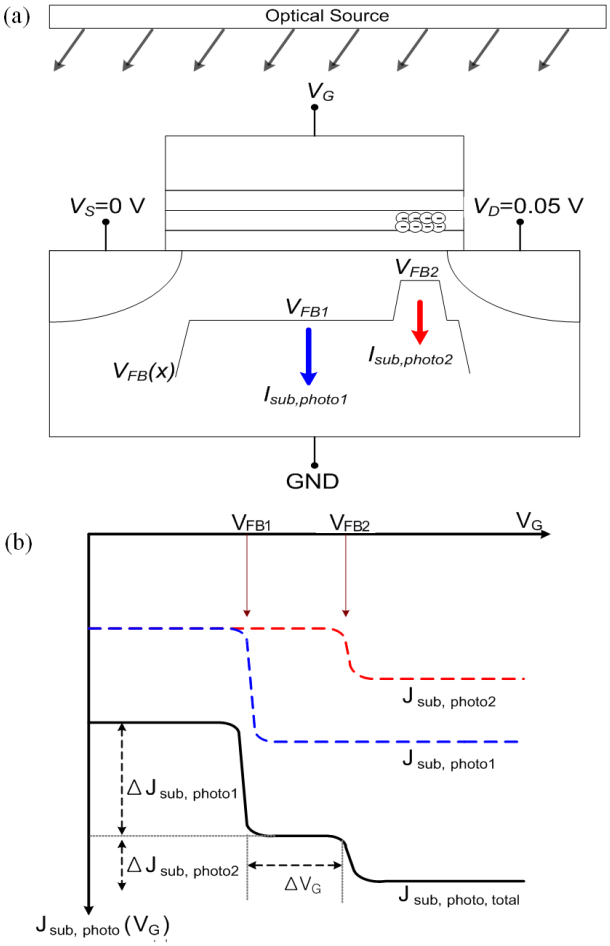

Fig. 4. (a) Schematic diagram of a locally-programmed CTF memory cell in photonic illumination. (b) Schematic diagram of the multi-step-like feature $J_{sub,photo}$.

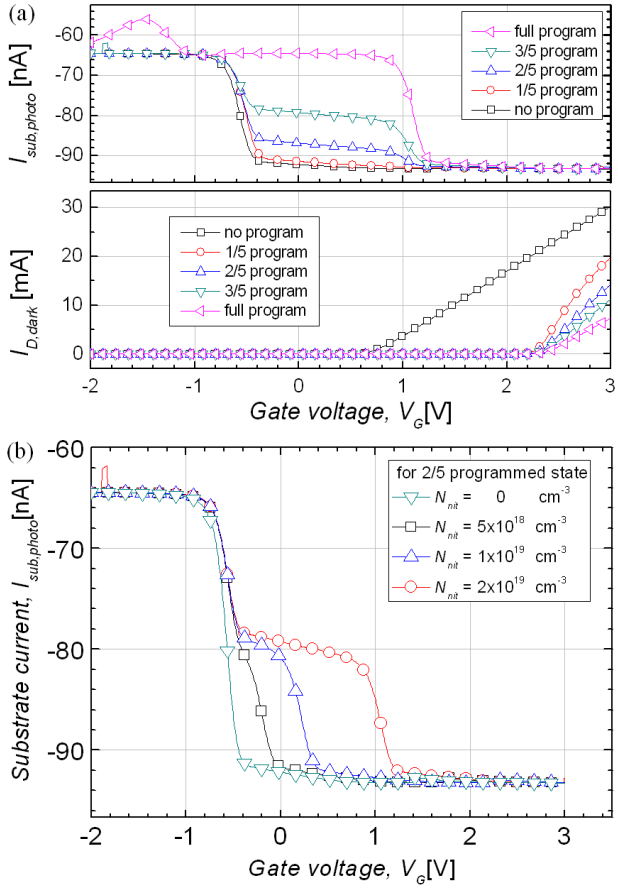

Fig. 5. (a) Simulation result for $J_{sub,photo}$ versus V_G in a locally-programmed CTF memory cell for various L_{prog} and $I_D - V_G$ curve in the dark state. (b) Simulation result for $J_{sub,photo}$ versus V_G in a locally-programmed CTF memory cell for various values of N_{nit}.

A schematic diagram of an n-type CTF memory device and the bias conditions are shown in Figure 4(a) and parameters needed to implement the photo-generation simulation are summarized in Table 2. The simulation is im-

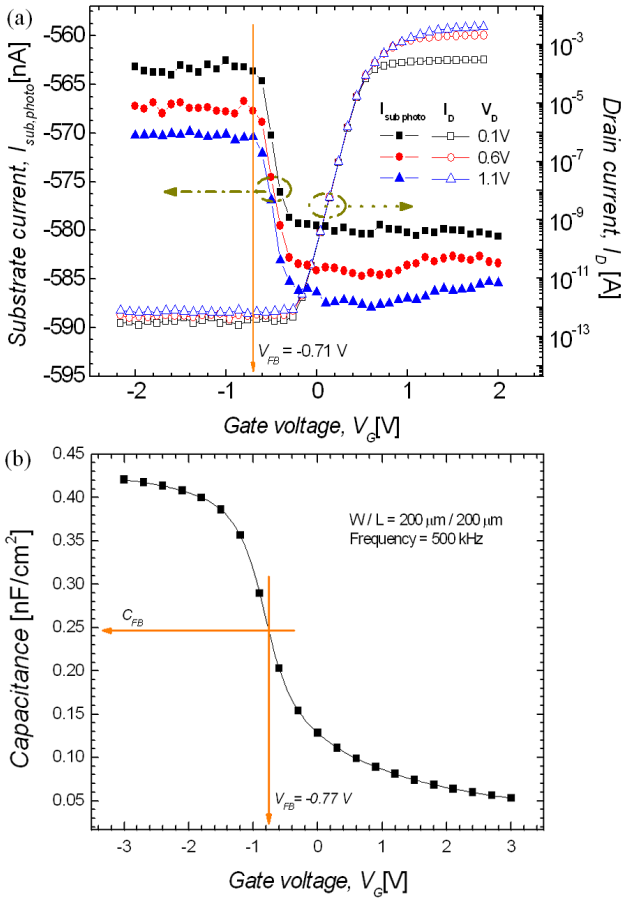

Fig. 6. (a) Measurement data for a n-channel MOSFET (W × L = 175 μm × 1.75 μm) with the drain bias dependence and the $I_D - V_G$ curve in dark state. (b) V_{FB} extracted from the C−V curve of the MOS by structure using Hillard's method (W × L = 200 μm × 200 μm).

plemented by varying the program region in the nitride layer, L_{prog}, from 0/5 (L_{prog}/L_g) to 5/5 (L_{prog}/L_g) with a uniform charge concentration of $N_{nit} = 10^{19}$ cm^{-3}.

Figure 5(a) shows the photo generation simulation results for a laterally nonuniform profile of electrons trapped in the nitride storage layer in a CTF memory. As shown in Figure 5(a), a multi-step response is clearly observed in the $I_{sub,photo} - V_G$ curve. The first transition points are the same in all cases because the intrinsic flat-band voltage, V_{FB1}, is unique for all cases while the $\Delta I_{sub,photo2}$ varies with the programmed region at the second transition points. As the programmed region is increased, the $\Delta I_{sub,photo2}$ is increased because the portion of $I_{sub,photo2}$ is increased. The programmed charge density dependence of $I_{sub,photo}$ is shown in Figure 5(b). As the programmed charge density increases, the second transition point shifts to the right due to the increased V_{FB2}. From Figure 6, we confirm that the second step's height is related to the programmed region and that the second step's width is related to the injected charge density.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The photo-generated substrate current, $I_{sub,photo}$ was measured for a n-channel MOSFET (W × L = 175 μm × 1.75 μm) and a semiconductor-oxide-nitride-oxide-semiconductor (SONOS) flash memory cell transistor (W × L = 10 μm × 0.22 μm, O/N/O layers: 40/40/40 Å) with an optical source (E_{ph} = 1.459 eV, ILX Lightwave Co., Model 7200), a cascade probe station and a HP4156C precision semiconductor parameter analyzer. In the n-type MOSFET, V_G is swept from −3 V to 3 V while V_D is varied. Not mentioned electrodes were grounded. The measurement substrate current, $I_{sub,photo}$ and its drain bias dependence with a drain current I_D are shown in Figure 6(a). As the drain bias increases, the magnitude of $I_{sub,photo}$ increases. The reason is that as V_D is increased, the photo-generated current in the drain depletion region, $J_{L,d}$, is also increased due to the extended depletion region. The transition point starts to have a large increasing gradient of $I_{sub,photo}$, which means that the V_{FB} point, is the same for all V_D bias conditions and is given by $V_{FB} = -0.71$ V. The C−V measurement results for a n-type MOS capacitor made under the same process conditions with an n-type MOSFET are shown in Figure 6(b). The V_{FB} extracted from the C−V curve using by Hillard's method is −0.77 V [9].

In the CTF flash memory cell transistor, V_G is swept from 0 V to 4 V with the drain bias fixed at V_D = 0.1 V and all other electrodes grounded. Not mentioned electrodes were grounded. Under the program conditions, channel hot electron injection (CHEI) (V_G = 5.5 V, V_D = 5.5 V, program time T_P = 1 ms) and Fowler-Nordheim (FN) (V_G = 13 V, $V_D = V_S = V_B$ = 0 V, program time T_P = 1 ms) tunneling are used. In the erase condition, both-sided band-to-band-assisted hot hole injection (HHI) (V_G = 0 V, V_D = 13 V, V_S = 13 V, erase time T_E = 1 ms) is used. Because the measured devices have ESD protection diodes, we could not apply only a negative voltage to the gate contact, so as shown in Figure 7(a), the flat-band voltage, V_{FB}, of the non-programmed region is not shown and only the second step is shown. After the CHEI program, we could see the difference in $I_{sub,photo}$ between the initial and the program states. The second step's height is increased and the width of the response is slightly increased after the CHEI program, meaning that the programmed region and the injected charges are increased. We increased the initial V_{FB} by using the FN program, then, both-sided HHI erase was performed. In Figure 7(b), $I_{sub,photo}$ in the FN programmed state is shown. In this condition, the first transition point V_{FB1} is shown due to the increased V_{FB1} by injected electrons. After both-sided HHI erase, the first transition point shifts left as much as 0.29 V because V_{FB1} is decreased by the injected holes. From there data, the injected volume charge density is 1.38 × 10^{18} cm^{-3} (C_{ono}

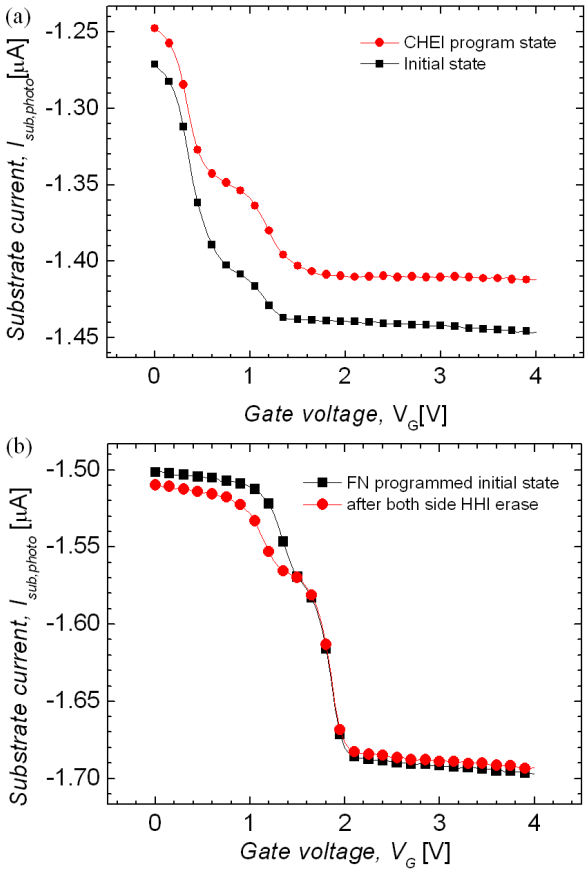

Fig. 7. (a) Measurement data for the n-channel CTF flash memory cell transistor (W × L = 10 μm × 0.22 μm, O/N/O layers: 40/40/40 Å). In the program conditions, CHEI (V_G = 5.5 V, V_D = 5.5 V and program time T_P = 1 ms) is used. (b) Measurement data for the n-channel CTF flash memory cell transistor (W × L = 10 μm × 0.5 μm, O/N/O layers: 40/40/40 Å). In the Erase conditions, both-sided HHI (V_G = 0 V, V_D = 13 V, V_S = 13 V, erase time T_E = 1 ms) is used.

= 3.45 × 10^{-7} F/cm^2, $t_{nitride}$ = 4 nm) and the lateral distribution range of both-sided injected holes is near 140 nm. Although we could not extract the accurate lateral distribution of trapped charges because of insufficient modeling of the lateral profiling, we confirmed that this method is able to detect the variation in the charge density and the lateral distribution. Further study is going on to extract a more accurate distribution of trapped charges.

V. CONCLUSIONS

In this work, we proposed a new extraction method for the local distribution of the flat-band voltage, V_{FB}, along the channel by using an optical source having a large energy compared to the silicon band-gap energy (1.12 eV). We clearly verified that the gate voltage starting to have a large increasing gradient of $I_{sub,photo}$ gives an accurate V_{FB} when using a TCAD simulation and analytic model. We applied this method to a CTF memory cell to extract the lateral profile of trapped charges along the channel in the nitride storage layer. Locally increased V_{FB} cause of by trapped charges induces a multi-step-like feature in I_{sub}–V_G curve. The second step's height is related to the programmed region and the second step's width is related to the injected charge density. Although we could not extract an accurate lateral distribution of trapped charges because of insufficient modeling of the lateral profiling, from the experimental results, we confirmed that this method is able to detect the variation in the charge density and the lateral distribution. Further study is going on to extract a more accurate distribution of trapped charges.

ACKNOWLEDGMENTS

This work was supported by the research program of Kookmin University in Korea. The CAD software was supported by the IC Design Education Center (IDEC).

REFERENCES

[1] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer and D. Finzi, IEEE Electron Dev. Lett. **21**, 543 (2000).
[2] W.-J. Tsai, N.-K. Zous, T. Wang, Y.-H. J. Ku and C.-Y. Lu, IEEE Trans. Electron Dev. **53**, 808 (2006).
[3] W. Chen, A. Balasinski and T.-P. Ma, IEEE Trans. Electron Dev. **40**, 187 (1993).
[4] S.-H. Gu, T. Wang, W.-P. Lu, W. Ting, Y.-H. J. Ku and C.-Y. Lu, IEEE Trans. Electron Dev. **53**, 103 (2006).
[5] A. Arreghini, F. Driussi, D. Esseni, L. Selmi, M. J. van Duuren and R. van Schaijk, Microelectronic Eng. **80**, 333 (2005).
[6] P. B. Kumar, P. R. Nair, R. Sharma, S. Kamohara and S. Mahapatra, IEEE Trans. Electron Dev. **53**, 698 (2006).
[7] E. Lusky, Y. S. Diamand, G. Mitenberg, A. Shappir, I. Bloom and B. Eitan, IEEE Trans. Electron Dev. **51**, 444 (2004).
[8] ISE TCAD: Synopsys Sentaurus Device User Manual, 1995-2005, Synopsys, Mountain View, CA.
[9] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. (Wiley, New Jersey, 2006), p. 328.