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Highly uniform carbon nanotube nanomesh network transistors

Sung-Jin Choi[1], Patrick Bennett[2,3], Dongil Lee[4], and Jeffrey Bokor[2,5] (✉)

[1] *School of Electrical Engineering, Kookmin University, Seoul 136-702, South Korea*
[2] *Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA*
[3] *Applied Science & Technology, University of California, Berkeley, CA 94720, USA*
[4] *Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, South Korea*
[5] *Materials Sciences Division, Lawrence Berkeley National Laboratories, CA 94720, USA*

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ABSTRACT

A new type of single-walled carbon nanotube (SWNT) thin-film transistor (TFT) structure with a nanomesh network channel has been fabricated from a pre-separated semiconducting nanotube solution and simultaneously achieved both high uniformity and a high on/off ratio for application in large-scale integrated circuits. The nanomesh structure is prepared on a high-density SWNT network channel and enables a high on/off ratio while maintaining the excellent uniformity of the electrical properties of the SWNT TFTs. These effects are attributed to the effective elimination of metallic paths across the source/drain electrodes by forming the nanomesh structure in the high-density SWNT network channel. Therefore, our approach can serve as a critical foundation for future nanotube-based thin-film display electronics.

1 Introduction

Single-walled carbon nanotubes (SWNTs) offer advantageous electrical properties, such as high intrinsic carrier mobility and current-carrying capacity [1–7]. Therefore, SWNTs have already been used extensively to obtain ballistic and high-mobility transistors [8–11] and integrated logic circuits [12–17]. Many types of SWNT network-based thin-film transistors (TFTs) also have been created by utilizing the numerous benefits of SWNTs, such as room-temperature processing compatibility [18], transparency [19], and flexibility [20–22]. Nevertheless, the mainstream SWNT TFT approaches still share a common drawback—the coexistence of both metallic and semiconducting nanotubes [23–27]. For digital electronic applications, this issue can be resolved by using preseparated semiconducting nanotubes produced by a density

Address correspondence to jbokor@eecs.berkeley.edu

gradient ultracentrifuge separation method [28, 29]. The selective removal of metallic nanotubes has been shown to dramatically reduce the leakage path, enabling the realization of high on/off ratios and high yields [17, 19, 21, 22, 30–34]. Numerous studies have focused on the electrical characteristics that result from the different separation rates of semiconducting enriched nanotube solutions (e.g., 90%, 95%, 98%, and 99% semiconducting nanotubes) which affect the performance of the SWNT TFTs. Based on those studies, improved electrical characteristics have been obtained as the percentage of semiconducting nanotubes in the solution is increased. However, the presence of a small amount of metallic nanotubes in the solution can still limit the performance of the TFTs when the density of the SWNTs in the network channel is sufficiently high to generate a sufficient drive current [27, 33–35]. In addition, the electrical characteristics of SWNT TFTs still lack uniformity, and no experimental studies have been performed to address this significant issue.

Herein, we present a new type of SWNT TFT structure which simultaneously affords high uniformity and enhances the on/off ratio of the devices by intelligent patterning of the network channel into a nanomesh structure. Our results demonstrate that even when constructed from a 90% semiconducting nanotube solution, the electrical characteristics of the fabricated nanomesh SWNT TFTs are significantly improved, resulting in a high on/off ratio and a high degree of uniformity. Thus, we expect that these SWNT TFTs are suitable for practical applications.

2 Fabrication process

Before nanotube deposition, a heavily doped silicon substrate with a 55-nm oxide layer (Si/SiO_2) was cleaned (using an O_2 plasma treatment) to make the surface hydrophilic. Next, the cleaned substrate was immersed in a poly-L-lysine solution (0.1% *w*/*v* in water; Sigma Aldrich) to form an amine-terminated adhesion layer and then rinsed with deionized (DI) water [21, 22]. Next, samples were immersed in a commercially available solution (0.01 mg/mL) of 90% semiconducting nanotubes (NanoIntegris Inc.) for 1, 3, or 14 min to form the network channel. The density of the SWNTs in the network increases with the deposition time and it becomes rapidly saturated. To achieve a sufficiently high-density SWNT network, therefore, we choose a deposition time of 14 min. We believe that a saturated high-density SWNT network could enable the uniformity issue in SWNT TFTs to be addressed. The samples were then rinsed with DI water and isopropanol and blow-dried in nitrogen. After the networks were formed, 30-nm Pd source–drain electrodes were deposited using e-beam evaporation followed by a lift-off process. Finally, because the nanotube thin films covered the entire chip, an additional step involving photolithography and O_2 plasma treatment was used to define the channel widths and remove unwanted paths. In all the devices, the gate width and length were fixed at 3 μm and 4 μm, respectively. Electrical tests of the fabricated devices were performed in air and at room temperature with no further passivation or annealing treatments.

3 Results and discussion

Figure 1(a) presents a schematic of the ordinarily fabricated SWNT TFT. The highly p-doped substrate is used as the back-gate. Figure 1(b) presents SEM images of the SWNT network that was fabricated with a deposition time of 14 min. From the images, we can conclude that the network film is uniformly deposited on the SiO_2 surface across the wafer. However, non-uniformly deposited SWNTs can be observed for shorter deposition time, such as 1 min and 3 min (Fig. S1 in the Electronic Supplementary Material (ESM)). Such non-uniformity can cause a

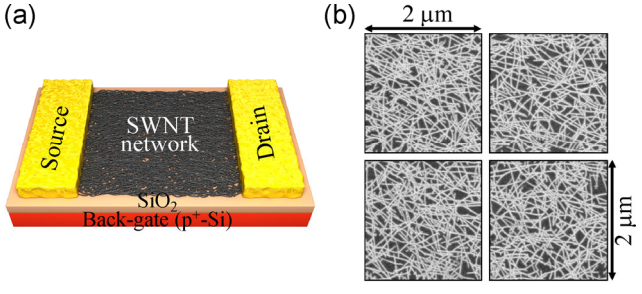

Figure 1 (a) Device schematic for the SWNT TFT constructed from a 90% semiconducting nanotube solution. (b) SEM images of SWNTs deposited on the SiO_2 surface (deposition time of 14 min) for different locations of the wafer.

variation in the number of connecting paths between source and drain (S/D) electrodes. Therefore, the high-density network film that is produced from the 14 min deposition is favorable for use in fabricating the nanomesh SWNT TFTs.

First, we measured the transfer characteristics of the drain current (I_D)–gate voltage (V_G) for the fabricated SWNT TFTs at a drain voltage (V_D) of –0.5 V (Figs. 2(a)–2(c)). We fabricated 144 devices for each network formation condition. As the nanotube deposition time was increased from 1 to 14 min to form the high-density network, the average on-state current, I_{ON}, defined at V_G = –10 V and V_D = –0.5 V, increased from 1.08 to 21.4 μA. In contrast, the on/off ratio, i.e., I_{ON}/I_{OFF} (the off-state current, I_{OFF}, is defined at V_G = 2 V and V_D = –0.5 V), exhibits the opposite trend, decreasing with increasing nanotube density in the network channel. This trend occurs because the probability of a metallic interconnection between the S/D electrodes increases at higher nanotube densities. The observed trend is consistent with prior reports and is straightforward to understand [30, 33, 35]. Therefore, the SWNT TFT entails an inherent tradeoff between I_{ON} and I_{ON}/I_{OFF}.

More importantly, the distribution of I_{ON} values

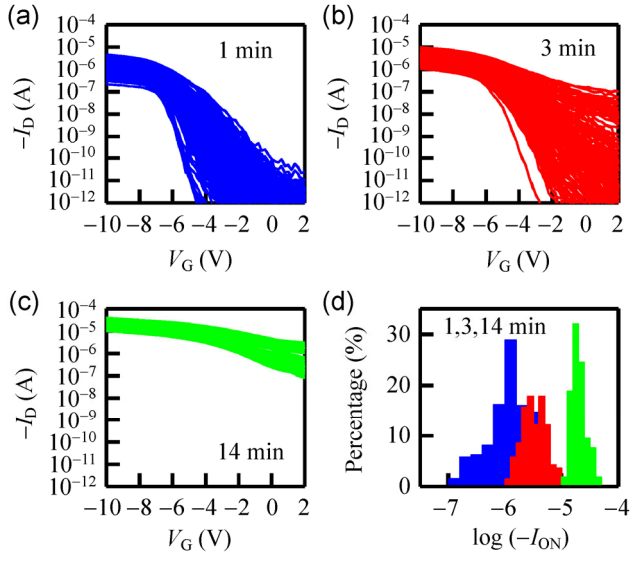

Figure 2 Transfer (I_D–V_G) characteristics of devices prepared with deposition time of (a) 1 min, (b) 3 min, and (c) 14 min at V_D = –0.5 V. (d) Histograms compiled from the transfer characteristics displaying the I_{ON} values for each condition. In all the devices, the gate width and length were fixed at 3 μm and 4 μm, respectively.

became significantly tighter as the nanotube density in the networks increased (Fig. 2(d)). Due to the statistical nature of the SWNT TFTs, some variations in I_{ON} values can be expected because of the variation in the number of connecting paths between the S/D electrodes. The devices with lower numbers of connecting paths, i.e., lower-density networks, are generally more affected by these variations than devices with higher numbers of connecting paths, i.e., higher-density networks. Thus, in the devices with the higher-density networks, the variation is expected to be reduced due to an averaging effect (Fig. S2 in the ESM) [36]. Thus, for short deposition time, such as 1 min, we observed large variations in I_{ON} values caused by the non-uniform network channel arising from the insufficient deposition time. In contrast, the distribution of I_{ON} values becomes more uniform as the deposition time is increased to 14 min. Therefore, the high-density nanotube network provides an important method of improving the device uniformity, but the metallic interconnections between the S/D electrodes should be effectively eliminated to obtain a high I_{ON}/I_{OFF}. Although we used a low semiconducting enriched nanotube solution (90%), this effect can be observed even in the devices that were constructed using higher semiconducting enriched nanotube solutions as well [30, 33].

To eliminate the metallic paths in the high-density nanotube network, we formed nanomesh structures in the network channels of SWNT TFTs fabricated with a deposition time of 14 min using e-beam lithography and an additional O_2 plasma etching process (Fig. S3 in the ESM and Fig. 3(a)). SEM and AFM were used to characterize the nanomesh structure (Fig. 3(b)). The resulting images exhibit periodically etched nanoholes over the entire network channel. The diameter of the etched holes and the smallest distance between two neighboring nanoholes were designed to be 50 nm and 212 nm, respectively. Although we used e-beam lithography to form the nanomesh structure in the network channel, block copolymer lithography and/or nanoimprint lithography could also be employed for low-cost, high-throughput production. These methods can also enable the design and fabrication of nanomesh SWNT TFTs and their circuits using standard semiconducting processing.

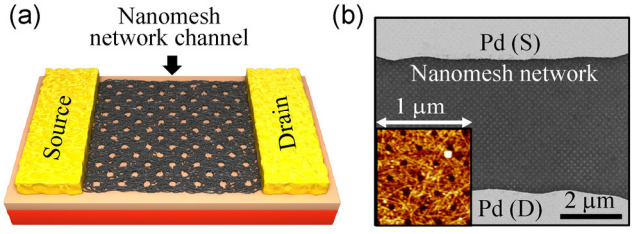

Figure 3 (a) Device schematic for the nanomesh SWNT TFT. (b) SEM image of the nanomesh SWNT TFT. Inset: AFM image of the nanomesh network channel. The diameter of the nanoholes in the nanomesh network channel is approximately 50 nm, and the smallest distance between the nanoholes is approximately 212 nm.

Figure 4 presents the electrical measurements of the nanomesh patterned high-density SWNT TFTs. The performances of the devices were more narrowly distributed at similar positions in the transfer characteristics while the I_{ON}/I_{OFF} ratio was increased considerably when compared to the unpatterned SWNT TFTs. This indicates that metallic paths resulting from the high-density network were effectively eliminated, while maintaining the high uniformity of the electrical properties due to the higher SWNT density. The I_{ON} values were distributed within a range of only 1 μA, but the average I_{ON} value of the nanomesh SWNT TFTs was reduced to 2.1 μA. This reduction might arise from the etched SWNTs, increased length of current paths, and/or decreased mobility (Fig. S4 in the ESM). However, we expect that the I_{ON} value could be improved by controlling the density and geometries of the nanomesh network. Further work is needed to elucidate the exact origin of the reduced I_{ON} in the nanomesh network SWNT TFT. To extract the mobility of the fabricated device, we simply used the parallel plate model to calculate the gate capacitance because it is hard to calculate the exact gate capacitance in the nanomesh SWNT TFTs. The extracted highest mobility of the devices is approximately 20 $cm^2 \cdot V^{-1} \cdot s^{-1}$. Strictly speaking, this value is not correct, because the parallel plate model overestimates the gate capacitance in general, resulting in underestimated mobility (Fig. S5 in the ESM). In addition, although small fluctuations are still observed in the subthreshold characteristics, the narrow distribution of I_{ON} values in either the linear or saturation regime is the most compelling characteristic when

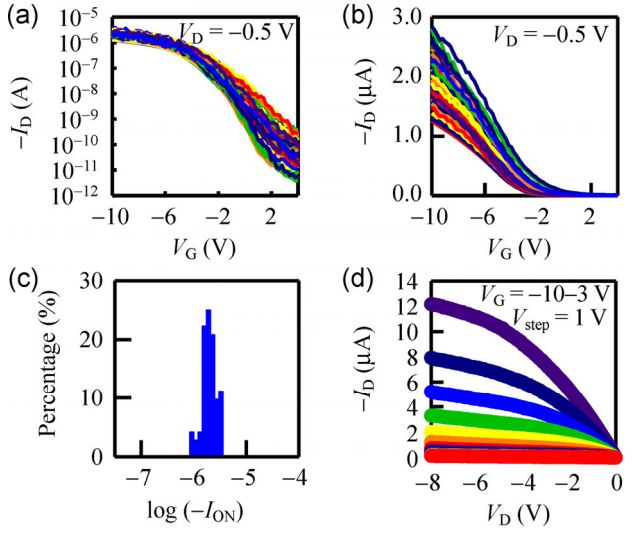

Figure 4 Transfer (I_D–V_G) characteristics ((a) log and (b) linear scale) of the nanomesh SWNT TFT at V_D = –0.5 V. (c) Histogram extracted from the nanomesh SWNT TFT illustrating I_{ON} values. (d) Output (I_D–V_D) characteristics of the nanomesh SWNT TFT for different gate voltages ranging from –10 to 3 V in 1 V step. In all the devices, the gate width and length were fixed at 3 μm and 4 μm, respectively.

considering the use of SWNT TFTs as driving transistors for display applications [19, 34].

To determine the exact origin of the improved characteristics of the nanomesh SWNT TFTs, we fabricated additional SWNT TFTs with varying distances between neighboring nanoholes (142 nm, 212 nm, and 354 nm) (Fig. 5(a)). Figures 5(b)–5(d) summarize the measurements of the different nanomesh SWNT TFTs as well as the unpatterned SWNT TFTs. Notably, the I_{ON}/I_{OFF} ratio of the SWNT TFTs is strongly affected by varying the distances between the nanoholes in the network. Reducing the separation between nanoholes increases the I_{ON}/I_{OFF} ratio by up to six orders of magnitude because of the finite probability that the metallic subnetworks are able to bridge the S/D electrodes can be further reduced [32, 34] It should be noted that the highly uniform electrical properties still remain unchanged despite the varying nanomesh structure, because changes in the nanomesh structure do not lead to significantly fewer connected paths (which would result in more electrical variations) [36]. Therefore, the ability to achieve highly uniform electrical characteristics with a high I_{ON}/I_{OFF} ratio in our nanomesh SWNT TFTs

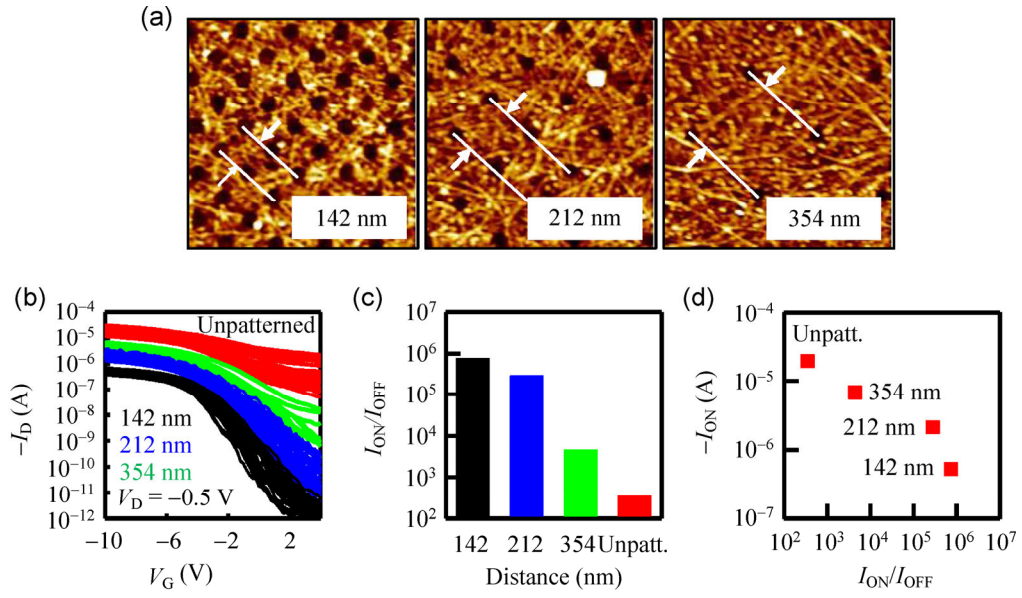

Figure 5 (a) AFM images of different nanomesh network channels with various distances between nanoholes (142, 212, and 354 nm). The diameter of the nanoholes in these nanomesh networks is approximately 50 nm. (b) Transfer (I_D–V_G) characteristics of the SWNT TFTs with various nanomesh conditions at V_D = –0.5 V. (c) I_{ON}/I_{OFF} ratio versus distance between neighboring nanoholes for each nanomesh condition. (d) Summarized results of I_{ON} versus I_{ON}/I_{OFF} ratios in the nanomesh SWNT TFTs with various distances between neighboring nanoholes. The results for the SWNT TFT with the unpatterned network channel are also shown in the figure as a control group. In all the devices, the gate width and length were fixed at 3 μm and 4 μm, respectively.

clearly highlights the advantages of the nanomesh network channel.

4 Conclusions

We have fabricated a new type of SWNT TFT with a nanomesh network channel that can effectively achieve a high I_{ON}/I_{OFF} ratio and high degree of uniformity. The I_{ON}/I_{OFF} ratio of the fabricated devices increases with decreasing distance between the nanoscale holes in the nanomesh network, while maintaining a high degree of uniformity. Therefore, we expect that such nanomesh SWNT TFTs will be suitable for use in future display applications.

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Electronic Supplementary Material: Supplementary material (uniformity of the deposited SWNTs on the surface, simulation results of the nanotube thin-film percolation network, detailed fabrication process of the nanomesh network, calculated resistance of the nanomesh channel, and extracted mobility) is available in the online version of this article at http://dx.doi.org/10.1007/s12274-014-0623-8.

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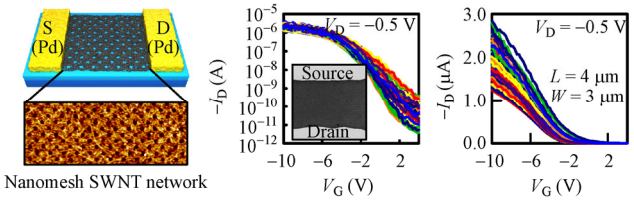

We have fabricated a new type of single-walled carbon nanotube (SWNT) thin-film transistor (TFT) structure with a nanomesh network channel from a preseparated semiconducting nanotube solution and simultaneously achieved both high uniformity and a high on/off ratio for application in large-scale integrated circuits.

Electronic Supplementary Material

Highly uniform carbon nanotube nanomesh network transistors

Sung-Jin Choi[1], Patrick Bennett[2,3], Dongil Lee[4], and Jeffrey Bokor[2,5] (✉)

[1] School of Electrical Engineering, Kookmin University, Seoul 136-702, South Korea
[2] Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA
[3] Applied Science & Technology, University of California, Berkeley, CA 94720, USA
[4] Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, South Korea
[5] Materials Sciences Division, Lawrence Berkeley National Laboratories, CA 94720, USA

Supporting information to DOI 10.1007/s12274-014-0623-8

1 Uniformity of the deposited SWNTs on a SiO_2 surface

AFM was used to investigate the uniformity of the SWNTs deposited across the wafer with different deposition time of nanotube solution. The SWNTs were not uniformly deposited on the surface when using deposition time of 1 min and 3 min. However, the uniformity improved with increasing deposition time. Non-uniformity of the SWNTs can cause variations in the number of connecting paths between the S/D electrodes. Thus, the I_{ON} values are likely to vary widely for a low-density network channel compared to a high-density network channel.

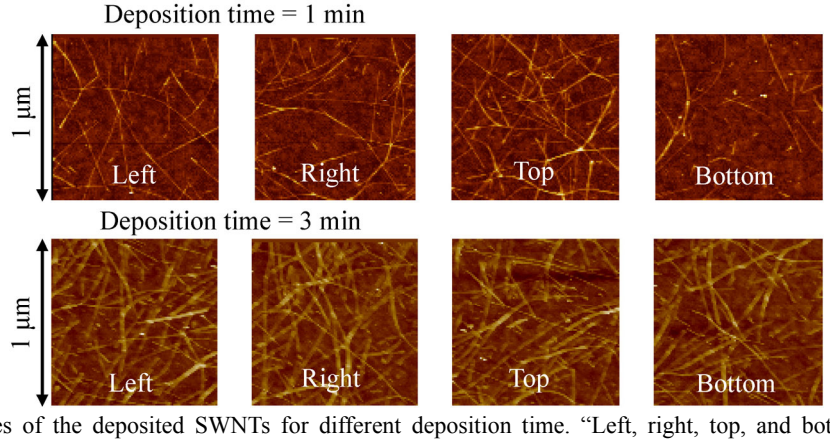

Figure S1 AFM images of the deposited SWNTs for different deposition time. "Left, right, top, and bottom" mean the different locations of the wafer.

2 Simulation of the nanotube thin-film percolation network

A numerical simulation was performed with various SWNT densities to assess the effect of SWNT density on the uniformity of the electrical characteristics. We generated random nanotube networks that are defined by the

Address correspondence to jbokor@eecs.berkeley.edu

density of nanotubes, nanotube length, channel length, and channel width. The green sticks indicate connected paths, and the blue sticks indicate non-connected paths between the S/D electrodes. For the low-density nanotube network, the connected paths are random for each simulation, indicating that the number of connected paths can vary significantly in low-density networks. In contrast, high-density nanotubes provide more uniform network results due to the averaging effect.

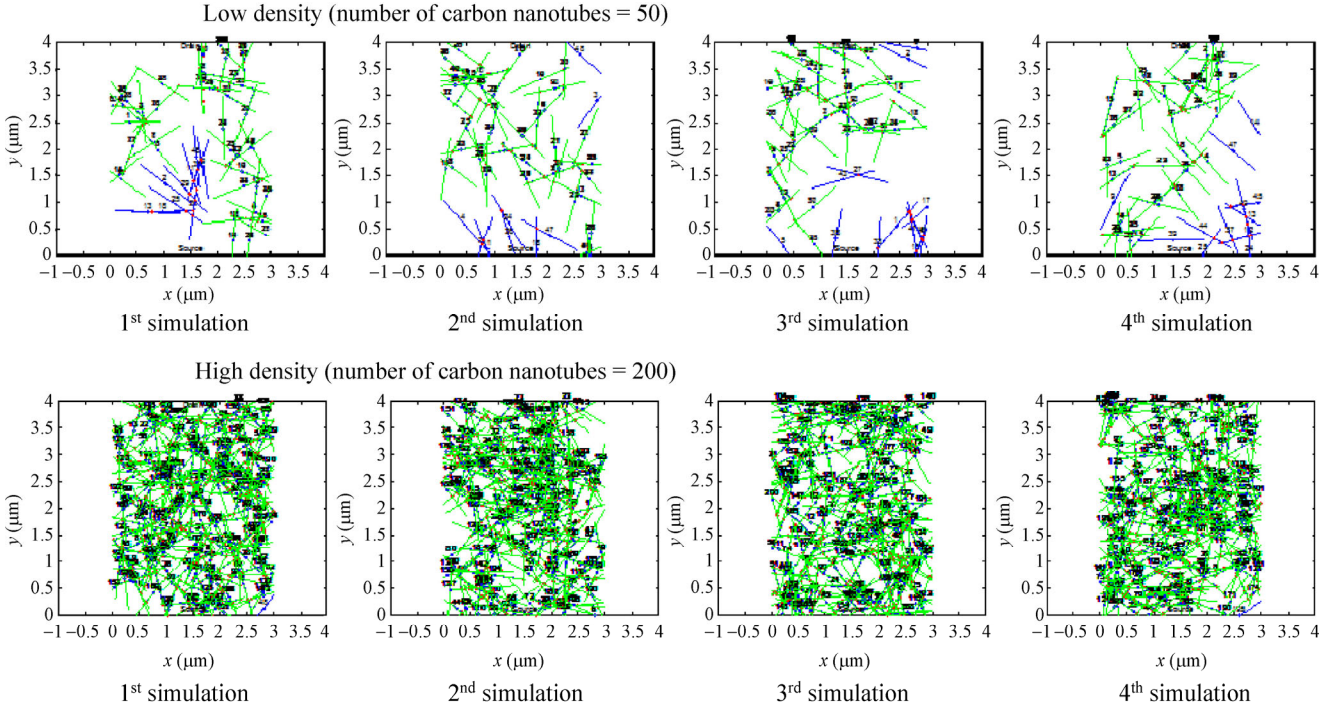

Figure S2 Simulation results for different nanotube densities. As the density increases, a uniform network channel can be formed by reducing the random effect.

3 Fabrication of the nanomesh network by e-beam lithography

First, poly(methylmethacrylate) (PMMA, 1 wt.% M_W 950k, 4 krpm spin) was spun on the SWNT network with a deposition time of 14 min and baked at 180 ˚C for 10 min. Next, PMMA was exposed to e-beam lithography (Crestec) and developed to pattern the nanomesh structure on the SWNT network, followed by PMMA removal using warm acetone (80 ˚C). The resulting SEM and AFM images are shown in Fig. S3.

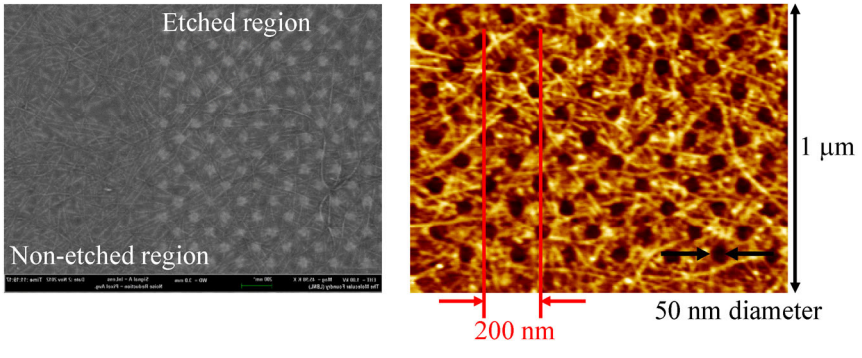

Figure S3 SEM and AFM images of the nanomesh network channel. The selectively etched holes were formed by elaborate e-beam lithography.

4 Increased resistance in the nanomesh channel caused by the etched network regions

In order to calculate the increased resistance due to the etched hole regions in the nanomesh channel, we model a thin film resistor with holes to evaluate how much the etched regions can affect the resistance of the film.

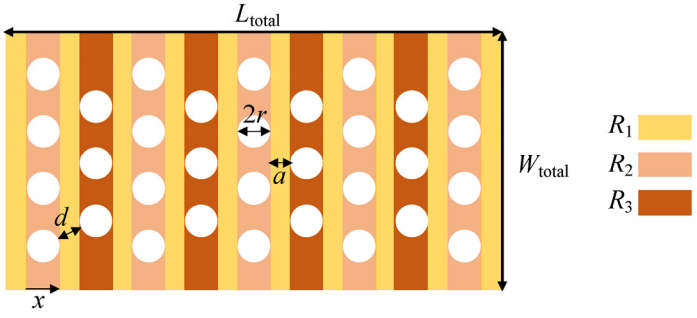

Figure S4(a) Schematic of the thin film resistor with holes. The total resistance of the film can be approximated as the series connection of R_1, R_2, and R_3.

The total resistance of the film is composed of the series connection of R_1, R_2, and R_3 components (i.e., $R_{total} = R_1 + R_2 + R_3$). For R_1 part, the resistance can be expressed as

$$R_1 = \frac{\rho}{t}\frac{L_{total} - 2rN_1}{W_{total}}$$

where t is the thickness of the film and N_1 is the number of R_1 components in the film. The R_2 and R_3 components can be obtained by

$$R_2 = \frac{\rho}{t}\frac{2r}{\frac{1}{2r}\int_0^{2r} W(x)\mathrm{d}x}\cdot N_2 = \frac{\rho}{t}\frac{2r}{\frac{1}{2r}(2rW_{total} - M\pi r^2)}\cdot N_2, \quad R_3 = \frac{\rho}{t}\frac{2r}{\frac{1}{2r}[2rW_{total} - (M-1)\pi r^2]}\cdot N_3$$

where $W(x)$ is the width of the film in R_2 or R_3 components, M is the number of holes in R_2 components, and N_2 and N_3 are the numbers of R_2 and R_3 components in the film, respectively. We assumed that the resistivity of each component is the same. Through the above equations, the resistance of the thin film with holes is obtained, as shown below.

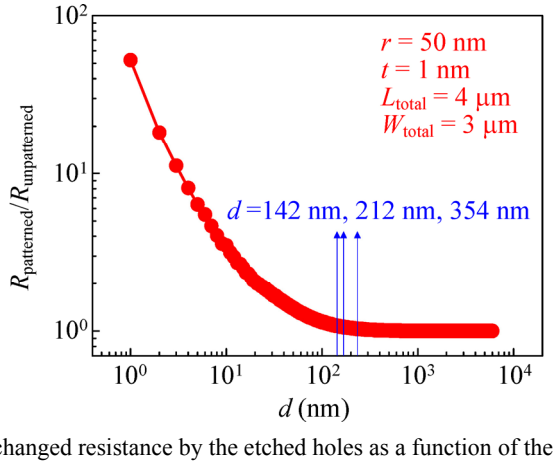

Figure S4(b) Calculated ratio of the changed resistance by the etched holes as a function of the distance between holes.

From the result, the increase in resistance caused by the etched holes is very small. Correspondingly, the reduction of I_{ON} values in nanomesh SWNT TFTs cannot be explained by the decrease in the channel area alone. Therefore, the increased resistance (i.e., reduced I_{ON}) of the nanomesh network SWNT TFT might arise from the etched nanotubes, increased current paths, decreased mobility, or other factors. The exact origin of the reduced I_{ON} in the nanomesh network SWNT TFT should be further investigated.

5 Extraction of mobility in the nanomesh SWNT TFT

To extract the mobility in the nanomesh SWNT TFTs, the exact gate capacitance is required but it is difficult to obtain because of the unique pattern of the nanomesh. Therefore, we simply use the parallel plate model to calculate the gate capacitance. The mobility can be extracted by the following equation

$$\mu = \frac{L}{V_D C_G W}\frac{dI_D}{dV_G} = \frac{L}{V_D C_G}\frac{g_m}{W}$$

The thickness of the gate dielectric in our devices is 55 nm, thus the gate capacitance per unit area is simply calculated by $\varepsilon_{ox}/t_{ox} = 6.2783 \times 10^{-8}$ F/cm^2. Therefore, the extracted highest mobility in our devices is approximately 20 cm^2·V^{-1}·s^{-1}.

However, the extracted mobility is somewhat underestimated because the parallel plate model generally overestimates the gate capacitance, especially when the network density is low. If we employ the cylindrical model for calculating the gate capacitance ($\left\{C_Q^{-1} + \frac{1}{2\pi\varepsilon_{ox}\varepsilon_0}\ln\left[\frac{\Lambda_0}{R}\frac{\sinh(2\pi t_{ox}/\Lambda_0)}{\pi}\right]\right\}^{-1}$ Λ_0^{-1}, where $1/\Lambda_0$ stands for the density of SWNTs, $C_Q = 4.0 \times 10^{-10}$ F/m is the quantum capacitance of carbon nanotubes, and R is the radius of nanotubes), higher mobility can be extracted according to the SWNT density in the network channel. However, the cylindrical model is also derived from the aligned arrays of SWNTs, and therefore it is expected to be only a qualitative guide, but not to hold quantitatively. The best way to calculate the gate capacitance is direct measurement, but this is difficult for our structure.

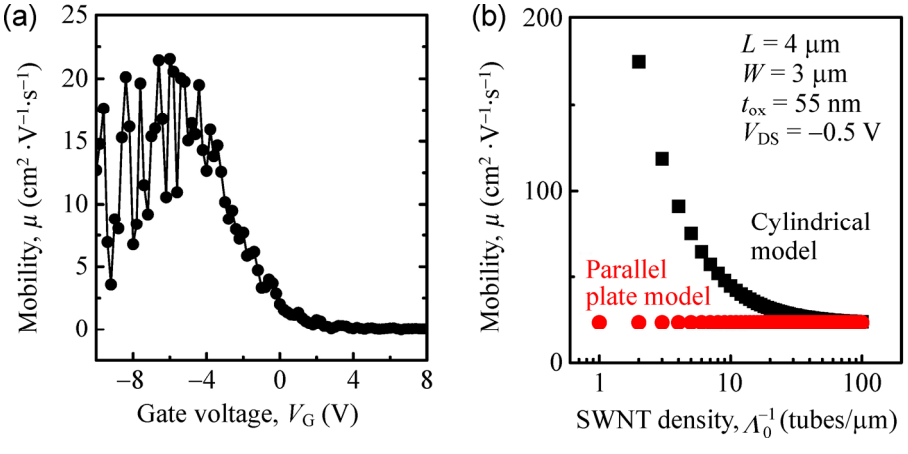

Figure S5 (a) The extracted mobility using the parallel plate model; (b) comparison of the extracted mobility through two methods for calculating the gate capacitance.